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Title: # General Specification For Printed Circuit Board Suppliers

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1 SCOPE

1.1 INTRODUCTION

This Specification supersedes the following specifications that have been discontinued or are obsolete:

HED Doc# PS164001 Rev A1 PC Board Supplier Requirements

This specification is based on the subtractive fabrication process utilizing Solder Mask over Bare Copper (SMOBC).

For Printed Circuit Boards (PCBs) manufactured to this specification by the supplier's various processes and utilizing varied raw material sources, the supplier is expected to select the proper copper thicknesses, base laminates, initial drill sizes, plating times, artwork compensation, etc., to assure that the finished product meets HED quality, dimensional and electrical requirements in their entirety.

Any modification to the design other than what is contained in this specification must be documented, submitted to HED and approved in advance of any change.

Specifications for RoHS (Restriction of Hazardous Substances) compliance and compatibility must be strictly adhered to.

1.2 RESPONSIBILITY

This specification defines minimum acceptable criteria for PCBs manufactured for HED; however, additional qualification may be applicable. It shall be the responsibility of the PCB supplier to inspect all artwork packages prior to commencing production, to verify that the PCB can be fabricated, netlist tested and inspected to all specification requirements.

Should discrepancies be detected during DFM, the supplier must contact HED Engineering for resolution. Any exception to this specification and / or artwork must have prior documented agreement from HED Engineering. All design queries must be resolved to consensus prior to production.

Initial quote and First Article report submission must disclose any outsourced processes (if applicable) and include laminate identification (manufacturer, type) and RoHS final finish specifics (type, manufacturer, alloy or chemistry).

After production First Article submission has been approved, no modification to design, construction, material, final finish or manufacturing site may be made without notification from supplier and subsequent approval from HED Engineering.

2 REFERENCE DOCUMENTS

The following specifications, to the extent referenced herein and at their latest revision, form a part of this document:

2.1 IPC SPECIFICATIONS (latest revision)

IPC-T-50F	Terms and Definitions
IPC-MF-150F	Metal Foil for Printed Wiring Applications
IPC-A-600F	Acceptability of Printed Boards
IPC-TM-650	Test Methods Manual
IPC - 9252	Guidelines and Requirements for Electrical Testing of Unpopulated Printed Boards
IPC-7721	Repair & Modification of Printed Boards & Electronic Assemblies
J-STD-003A	Solderability Tests for Printed Boards
IPC-SM-840C	Qualification and Performance of Permanent Solder Mask
IPC – 4101B	Specification for Base Materials for Rigid and Multilayer Printed Boards
IPC-4554	Specification for Immersion Tin Plating for PCBs
IPC-6011	Generic Performance Specification for Printed Boards
IPC-6012B	Qualification and Performance Specification for Rigid Printed Boards
IPC-6013	Qualification and Performance Specification for Flexible Printed Boards
IPC-6016	Qualification and Performance Specification for High Density Interconnect (HDI) Layers or Boards

2.2 THE AMERICAN SOCIETY OF MECHANICAL ENGINEERS

ASME Y14.5M	Dimensioning and Tolerancing (1994)

2.3 UNDERWRITERS LABORATORIES DOCUMENTS

UL-796	Standard for Printed-Wiring Boards

2.4 ORDER OF DOCUMENT PRECEDENCE

In case of conflict with documentation, the following order shall apply:

Purchase Order
Assembly Parts List (BOM), Latest Revision (if supplied via PO)
Appendix Sections of this document
PCB Fabrication Drawings
IPC-6011 / IPC-6012A / IPC-RF-245
IPC-A-600F
ASME Y14.5M-1994 or Coordinate Dimensions

3 FINISHED BOARD ACCEPTANCE REQUIREMENTS

This section defines the finished PCB acceptance requirements. HED requirements that differ from established industry standards are defined in this section.

UNLESS otherwise stated on the Purchase Order, drawing or this specification, all PCBs shall meet CLASS 3 REQUIREMENTS as defined in IPC-6012B / IPC-A-600F / J-STD-003A (latest revisions).

3.1 FIRST ARTICLE INSPECTION REQUIREMENTS

First Article Inspection submission is required for first prototype and production shipment of each new part number, existing part numbers that have undergone revision change affecting fit, form or function or existing part numbers being fabricated at a different, HED approved, manufacturing location.

The First Article Inspection submission shall document and include the following lot representative items:

- Dimensional and fabrication drawing note verification
- Micro-section report (defining Cu thicknesses at critical locations) and samples.
- 100% netlist electrical test verification
- Ionic contamination test results / certification
- Impedance test results and coupons
- Laminate certification identifying manufacturer & product number and verifiable compliance. Lot number must be attainable if requested.
- RoHS compliant finish certification – type, manufacturer, chemistry, or alloy (as applicable). Lot representative lead free solder (LFH) or immersion silver (IAg) thickness verification results.
- Solderability verification to J-STD-003A, Class 3 / Category 3 / Test Method C (Send tested samples)
- Additional process monitoring evidence may be required by HED (defined during Early Supplier Involvement (ESI) discussion).

This package is required to release PCBs into production and must be received in parallel with the initial shipment, either separately or with production boards (carton containing FA must be clearly identified for Receiving Inspection processing).

3.2 LAMINATE REQUIREMENTS – UL and IPC

3.2.1 RoHS COMPLIANCE

If “RoHS Compliance Required” or “High Temperature Laminate” is specified on the PCB fabrication drawing, the following criteria must be followed to assure use of correct HED specified laminate.

If the design specifies any of these three attributes:

- Ten layer or more
- Two ounce or greater inner layer copper
- Nominal overall thickness of .070" or greater

The laminate base materials must meet or exceed criteria defined in IPC-4101B / 99 or IPC-4101B / 124 specification sheets and have a minimum of 170 degrees C Tg (glass transition temperature) and 340 degrees C Td (decomposition temperature).

If the design does not include any of the three attributes listed above, then the laminate base materials must meet or exceed criteria defined in IPC-4101B / 99 or IPC-4101B / 124 specification sheets.

For high temp laminates that meet all requirements, but are not yet HED recognized and approved, provide appropriate verification data and send as DFM Engineering query to HED Engineering for review and disposition. Sample submission may be required before approval for use.

Current HED Evaluated and Approved High Temperature Laminates

Polyclad 370HR
Polyclad 370 Turbo
Isola IS-410
Nelco N-4000-11

No change can be made without HED approval. Any parametric or supplier change of laminate materials must be pre-approved by HED Engineering. Additional requirements may be found on the specific fabrication drawing.

Fabrication drawing requirements take precedence over this specification.

3.2.2 NON-RoHS COMPLIANCE

If RoHS Compliance or High Temperature Laminate is NOT specified on the PCB fabrication drawing, FR-4 laminate meeting IPC 4101B / 21, 94V-0, 130C Tg minimum, with soldering limits not less than 260ºC (500ºF) for 4 (four) seconds shall be used.

It shall be the responsibility of the fabricator to assure that all PCBs are UL Component Recognized (UL Guide ZPMV2); compliant to UL796 Direct Support of Current-Carrying Parts, with a Maximum Operating Temperature (MOT) of not less than 130°C, with the exception of rigid-flex designs (105 C).

A UL Performance Level Category (PLC) of 3 or less ((synonymous with a CTI (Comparative Tracking Index) of 175 or greater)) is required for all PCBs and shall be identified as such on each individual PCB and readily auditable through the supplier's UL ZPMV2 file. ***NOTE:*** CTI column in supplier's UL ZPMV2 file must have an asterisk

(*) or (3 or less) in the appropriate PCB 'Type' classification for the supplier to have authority to mark CTI value on pcbs. A dash (-) in the CTI column signifies that the supplier has not received UL authorization to mark CTI value on boards within that type classification. Contact UL or HED for clarification as needed.

3.2.3 UL COMPLIANCE

It is the supplier's responsibility to assure that the correct UL designation matching these requirements is marked on each individual PCB, or if not possible due to size constraint, readily auditable through the supplier's UL ZPMV2 file. UL compliance implies recognition of the PCB manufacturing process as well as the PCB materials.

3.3 IPC-6012B / IPC-T-50F EXCEPTIONS

3.3.1 The terms and definitions listed below are exceptions to IPC-T-50F:

Coordinate Tolerance - A method of tolerancing in which the tolerance is applied directly to linear and angular dimensions, usually forming a rectangular area of allowable variation.

Panelization Carrier - Base material that surrounds or partially surrounds one or more printed circuits arranged in rows and /or columns for assembly purposes. This material may incorporate features used to enhance the assembly process.

BOM - The Bill of Materials that lists the part numbers and appropriate revision of the tools and/or specifications required to engineer and manufacture a PCB.

Deviation - A one-time, Purchase Order specific, authorized deviation to a specification or drawing. All deviation requests must be formally submitted to Purchasing and approved by HED prior to shipment.

The Following Sections "X.X.X" Are Exceptions to Equivalent Sections of IPC-6012B:

"3.2.6 Metallic Platings and Coatings"

Change Table 3-2: "Gold (min) for edge-board connectors and areas not to be soldered" requirement to 0.8µm or 30 micro-inches [0.00003 in] and Remove requirement for Note 3 below Table 3-2.

"3.2.6.1 Electroless Depositions and Conductive Coatings"

Add the following: "Conductive coating processes shall not be utilized without prior approval from HED Engineering."

"3.2.6.4 HASL Finish"

Add the following: "The HASL finish (SnPb and SN100CL LFH) should be bright and shiny with a maximum thickness of .001 in. (.0254 mm)." Minimum coating requirement shall be 80 micro-inches (2 microns). Via holes smaller than .018" (0.457 mm) nominal finished diameter may be plugged during the HASL process.

"3.2.6.7 Approved RoHS Compliant Surface Finishes"

If a design requires a RoHS compliant finish, this will be specified with a fabrication drawing note stating "RoHS Compliance Required". The supplier will utilize the approved, supplier specific finish/chemistry that will have been derived from Early Supplier Involvement (ESI) discussion with HED Engineering. Some drawings will define specific finish requirements, which take precedence over this specification.

Surface finishes must comply with solderability requirements.

The Order of Preference for HED approved RoHS finishes is:

Lead Free HASL (LFH) – the only HED approved alloy is Nihon-Superior SN100CL. Each shipment of LFH product shall include (1) lot representative, Class 3 compliant micro-section and (1) solder sample for HED evaluation. Additional process control verification data may be required by HED, and these parameters will be defined during ESI discussion.

Immersion Silver (IAg) – Immersion Silver is a RoHS finish that will be reduced in use as supply base migrates to LFH. Each shipment of IAg finished pcbs shall include XRF test data verifying lot average Ag thickness of greater than / equal to one micron (40 microinches) along with successful J-STD-003A, Class 3 / Category 3 / Test Method C solderability test results and sample. IAg finished product must be no more than three (3) months old when received at HED.

"3.2.6.8 Non RoHS finish requirements"

If there is no drawing note pertaining to final finish, SnPb HASL should be utilized. Additional requirements may be found on the fabrication drawing. Contact HED for clarification, if needed, prior to commencing production.

"3.2.10 Marking Inks"

Remove the following in first sentence: ", and shall be specified in the procurement documentation" *and add the following:* "The preferred marking ink shall be white in color." "Component legend registration shall be + .005 (0.127 mm). Component legend must be legible. Minor skipping or smearing which does not affect legibility or solderability is acceptable. Legend artwork shall not be modified without prior documented approval from HED Engineering. **Ink is NOT permitted on surface mount land areas.** HED Engineering shall approve exceptions.

"3.3.6 Solderability"

Add to last sentence in Paragraph 1: "...and shall meet the requirements of J-STD-003A, Class 3 / Category 3 / Maximum Coating Durability."

"3.3.8 Edge Board Contact, Junction of Gold Plate to Solder Finish"

Delete this section. Add the following: "The junction of the solder mask and contact plating shall not exhibit exposed copper or solder at the interface. Contacts shall always be plated to the solder mask junction or be overlapped by solder mask."

"3.4 Board Dimensional Requirements"

Add the following after the first paragraph: "Copper entity locations on the PCB must be correct to Gerber Data to + .003" (0.076 mm) for panel sizes up to 10.0 x 14.0" (254mm x 355.6mm). Outer layer etched feature to adjacent etched feature tolerance must be +/- .001" (.0254mm). Hole to feature tolerance shall be +/- .003" (.076mm). Hole to hole tolerance shall be +/- .003" (.076mm). Inner layer registration to drilled hole tolerance shall be +/- .005" (.127mm). Mask to feature tolerance shall be .003" (0.076mm).

"3.4.2 Annular Ring and Breakout (Internal)"

See APPENDIX A: ARTWORK ENHANCEMENTS for acceptable enhancement requirements.

"3.4.3 Annular Ring (External)"

See APPENDIX A: ARTWORK ENHANCEMENTS for acceptable enhancement requirements.

"3.4.4 Bow and Twist"

Delete the following in the first sentence: "the printed board shall have a maximum bow and twist of 0.75% for boards that use surface mount components and 1.5% for all other boards". *Add the following:* "the printed circuit board shall have a maximum bow and twist of 0.007" per inch in any direction (.7%) as measured per IPC-TM-650 Procedure 2.4.22, Revision C."

"3.5.2 Conductor Spacing"

Add the following: "A 20% or 0.002" (0.0508mm) reduction, whichever is less, in minimum conductor spacing is allowable in isolated areas due to conductor material edge roughness, copper spikes, etc."

"3.5.3.1 Conductor Width Reduction

Add the following: "Any Combination of edge roughness, nicks, pinholes, and scratches exposing base material shall not reduce the conductor width by more than 20% or 0.002" (0.0508mm), whichever is less, of the minimum value."

"3.6.2 Requirements for Micro-sectioned Coupons or Production Boards"

Correct the end of the first sentence: …and 3.6.2.1 through 3.6.2.15.

"3.6.2.6 Smear Removal"

Add the following: "Epoxy smear is unacceptable at both sides of the hole wall when viewed by cross-section. Epoxy smear is acceptable if 10% or less of the conductive interface thickness and/or if 10% or less of the circumference exhibits this condition."

"3.6.2.11 Minimum Internal Layer Copper Foil Thickness"

Add the following: "If not specified on the drawing the inner-layer copper foil thickness is 1.0 oz. copper."

"3.6.2.12 Minimum Surface Conductor Thickness"

Add the following: "If the surface copper thickness is not specified on the drawing, the nominal copper thickness shall be 2 oz. finished." This shall be derived from 1 oz. starting copper with 1 oz. copper deposition. No additional copper shall be added to usable board area without HED Engineering approval.

"3.6.2.14 Dielectric Thickness"

Delete this section and add the following: "Unless otherwise specified on the fabrication drawing, the minimum dielectric thickness for all design classifications shall be 0.0035" (0.09mm). The minimum number of glass cloth layers between conductive layers shall be two. When microvias are used, Resin Coated Copper (RCC) or single ply laminates may be used as specified in the procurement documents.

Thin Laminates (PCBs with a finished thickness of less than 0.050" (1.27mm)) may have minimum dielectric spacing of 0.002" (0.051mm) provided low profile copper foils are used. The minimum number of glass cloth layers between conductive layers shall be one."

"3.8 Solder Resist (Solder Mask) Requirements"

Add the following: "Solder mask is required on all PCBs, shall be applied over bare copper and shall be green in color. HED must qualify all solder mask materials.

ACCEPTABLE SOLDER MASKS

Vantico Probimer 77MA
Enthone DSR3241MD
Enthone DSR3241 CR
Taiyo PSR4000BN
Taiyo PSR4000MH
Taiyo PSR4000MP
Tamura DSR-2200TL-05M
Tamura DSR 2200 CCD CD-13B (by HED approval only)
Tamura DSR 330-C10-19SM (by HED approval only)
Probimer 65

"3.8.1 Solder Resist Coverage"

Add the following: When a design specification has no soldermask apertures for a via on both sides, the supplier shall fill or plug those vias with soldermask or non-conductive

epoxy before final finish (full plug process). Some designs may require use of conductive epoxy as plug material – this will be specified on the applicable fabrication drawing. The supplier must select the fabrication parameters that provide HED with full length, void and contaminant free plugs that will not dislodge during thermal cycling (260C maximum) associated with SMT assembly. For designs with soldermask apertures smaller than the copper feature size (encroaching on ring or pad), the supplier is not to modify. No via tenting or via plugging after final finish is permitted. Design queries must be communicated and resolved prior to commencing fabrication. Contact HED for clarification / resolution, as needed.

"3.8.3 Solder Resist Thickness"

Delete sentence 1. Add the following: "Soldermask thickness shall be less than the combined copper and final finish thickness (and therefore lower than component pad surfaces). Applying more than one coat of soldermask to either side to the PCB is not permitted, without prior documented HED approval. See "3.12 Repair" for acceptable soldermask touch-up." Regardless of method of application, soldermask thickness should not exceed 1.5 mils (0.038 mm). The minimum thickness requirement shall be 'no exposed copper prior to final finish'.

"3.9 Electrical Requirements"

Add the following: "All PCBs must be 100% tested for continuity and isolation per IPC – 9252 Class 3 requirements, except that the continuity parameter will be 20 ohms. All exposed copper on secondary (solder) side of each board should be included in test (net midpoints). HED provided net lists (IPC-D-365) shall be utilized for ET program creation. Each PCB should be identified as having been successfully tested (stamp or other approved marking). For those PCBs that cannot be individually stamped or marked (due to size / artwork constraints), the panelization carrier (waste area) will bear this electrical test identification.

"3.9.1 Dielectric Withstanding Voltage"

Dielectric Withstanding Voltage testing is not required unless specified on the part number drawing.

"3.9.2.2 Insulation Resistance"

Add the following: "The insulation resistance between conductors shall be greater than 10 meg ohms in all cases."

"3.10 Cleanliness"

Add the following: "The contamination level shall not be greater than an equivalent of [1.09ug/cm2 (7.00 ug/in2)]"of sodium chloride."
In addition, add the following: "Alternatively, ionic contamination may be assessed using Ion Chromatography (IC) per IPC-TM-650, method 2.3.28.

The allowable contaminant levels by this method are as follows:

Chloride: 0.54 µg/cm2 (3.50 µg/in2) maximum
Bromide: 2.33 µg/cm2 (15.00 µg/in2) maximum

Results as determined by IC shall take precedence over results as determined by Resistivity of Solvent Extract (ROSE). Lot acceptance shall not be determined by IC results which conflict with ROSE results, but corrective action may be requested by HED to bring fabrication process into compliance with IC requirements."

"3.10.1 Cleanliness Prior to Solder Resist Application"

In last sentence, substitute the following: "[1.09µg /cm^2 (7.00 µg / in^2)]" for [1.56 µg / cm^2 (10.06 µg /in^2)]."

"3.12 Repair"

Add the following: "All repairs not defined here must have prior documented approval by HED Engineering.

The following repairs are acceptable repair methods and will not require prior approval:

Conductor-Conductor Shorts - Repairs of conductor to conductor shorts are permitted on both outer and inner layers provided minimum space widths are met in all cases.

Gold Edge Contact Defects - Gold edge contacts shall not exhibit scratches, voids, solder on the contact surface, etc., and shall be repaired in accordance with IPC-7721 and Procedure 4.6.1, "Edge Contact Repair, Epoxy Method or IPC-7721 Procedure 4.6.3, Edge Contact Repair, Plating Method.

Key Slot Repair - Incorrect or damaged key slots shall be repaired in accordance with IPC 7721, Procedure 3.4.1 Key and Slot Repair, Epoxy method for damaged/minor repairs and 3.4.2, Key and Slot Repair, Transplant Method for incorrect slots.

Solder Mask Touch-Up - Brush touch-up with solder mask of exposed circuits, solder mask skips or other discontinuities are acceptable provided the quality or appearance is not compromised and they meet the following criteria:

1. Solder mask skips and pin holes exceeding 0.020" diameter are not 'touch-up' eligible
2. Solder mask skips and pin holes shall not exceed more than one defect per 10.0 in2.
3. Solder mask touch-up should not exceed 0.001" above original solder mask height.
4. Solder mask touch-up must pass adhesion testing. Brush touch-up with solder mask is unacceptable in areas where SMT components will be placed."

"3.12.1 Circuit Repairs"

Add the following: "A maximum of three circuit repairs per side are allowed. Weld repairs are not permitted on inner layers."

"4.2 Acceptance Tests"

Add the following: "Acceptance micro-section testing shall be performed as specified in Tables 4-2 and 4-3 of IPC 6012B to the requirements and panel lot sizes defined for Class

2 product. This is the only deviation from IPC Class 3 specifications allowed in this document.

Demonstrated evidence of optimal chemical and fabrication process control may result in microsection test quantity reduction, as determined by / approved by HED Engineering. Contact HED to obtain specific requirements. No reduction in micro-section test quantities is permitted without prior HED Engineering approval.

HED reserves the right to verify compliance at any time and/or to modify these requirements based on Supplier's quality performance.

3.4 PCB THICKNESS

3.4.1 Thickness Requirements

Unless otherwise stated on procurement documentation, 2-4 layer designs shall have a thickness tolerance of + 10%, while designs having greater than 4 layers shall have a thickness requirement of + 12%.

3.4.2 Method of Measurement

The overall thickness of the PCB shall be measured at the center of the gold contacts. On PCBs that do not have gold contacts, an area having soldermask over copper on both outer layers near the edge of the PCB shall be used.

3.5 GOLD CONTACT REQUIREMENTS

3.5.1 Gold/Nickel Plating Porosity

The gold and nickel platings must not exceed 30 pores per square centimeter when measured in accordance with IPC-TM-650, number 2.3.24.2, Porosity of Metallic Coatings on Copper-Base Alloys, and Nickel (Nitric Acid Vapor Test). Method 3, Nitric Acid Vapor - Gold on Nickel shall be the method used.

3.5.2 Contact Acceptability

The following requirements shall be met:

- All edge finger connectors shall be gold plated unless otherwise specified.
- The contact area (area of an edge finger connector or key pad that is not covered by solder mask) shall not exhibit evidence of delamination, burrs, solder, routing slivers, plating slivers or burned and/or rough plating.
- The plating surface, when examined without magnification, shall appear to be smooth, continuous and uniform in appearance. When examined with 10X magnification, the contact shall ***NOT*** contain:

1. More than one pit or dent whose greatest dimension is 0.01" (0.254mm) maximum

2. Exposed nickel or copper plating

3. Blisters

4. Scratches greater than .005" (0.127mm) wide

5. Nodules whose greatest dimension is over .005" (0.127mm) or whose presence increases the PCB thickness when measured at the contact area beyond the limits established in this specification

6. Copper burrs as a result of scoring

3.6 FINAL FABRICATION

3.6.1 Edge Condition

Edge condition acceptance shall be per IPC-A-600F, Section 2.1.1, acceptable.

3.6.2 Keying Slots

Keying slots shall not cut into or reduce any conductors or contacts. Dimensions refer to the maximum depth of the slot and not the center point of the router tool.
Designs having "crop marks" used to identify the location of a key slot shall have the crop marks removed when keying slots are not required in that location.

3.6.3 PCB Edge Chamfer

Chamfering is required on all PCBs having gold edge contacts, (unless fabrication drawing specifies differently) and must extend the entire length on both sides (top and bottom) of the gold fingers per Figure 2: PCB Edge Chamfer. The chamfer must be a smooth surface per section PCB Edge Chamfer. If not specified on the drawing, see Figure 2: PCB Edge Chamfer below for default chamfer requirements.

3.6.4 Panelization Carriers (Waste area)

The supplier may add copper thieving and / or additional holes for registration testing, etc. to the panelization carrier. Thieving must not be located within .090" (2.29mm) radius of fiducial locations.

Copper voids and scratches in the copper thieving areas that do not affect these features are permitted.

3.6.5 Bad Boards (X-Outs)

Unless specified on the fabrication drawing or with prior approval from HED Engineering, defective PCBs in panelized designs (X-outs) are unacceptable.

3.7 PCB REVISION IDENTIFICATION

3.7.1 Revision Marking

If not already marked in etch or silkscreen and embedded in the PCB data files. Suppliers are expected to identify each Printed Circuit Board in a clear, legible, permanent manner with the PO specified part number immediately followed by the revision level. The revision placed on the PCB must match the "Engineering Change Level (ECL)"identified on the Purchase Order.

All markings shall be 0.080-0.130" (2.03-3.30mm) high and are routinely located on the secondary (solder) side of the PCB.

Silkscreened identification is preferred, but most designs have this information included in the copper artwork. Certain designs prohibit the addition of copper to usable board area – check specific part number drawing notes for this requirement.

Should the supplier encounter compliance difficulty or have questions on part marking, contact HED for clarification / resolution.

3.8 SUPPLIER IDENTIFICATION

3.8.1 Location Requirement

Typically, a 0.500" (12.7mm) square box on the secondary side is provided for permanent marking of the UL accepted company identification (supplier's UL logo), date code, board technology classification, CTI and UL 796 compliance mark (as applicable). If a box is not provided, the supplier shall place the UL logo in the most convenient location of the usable PCB area. A minimum distance of 0.216" (5.5mm) from any pad or trace shall be maintained if etch is used for marking. For multi-up panels, each PCB shall have a UL logo.

All Supplier stamps, and/or etched identifiers are to be located on the secondary (solder) side of PCB. If not possible, the primary side may be used.

For U.S. Customs purposes, suppliers outside North America shall identify the country of origin by applying "Made in (Country of origin)" on the PCB component side. Preferred locations are as follows:

- On the panelization carrier
- If no panelization carrier exists, ***UNDER*** a large component location

3.8.2 Date Code

The date code may be in copper or in legend ink and shall reflect the week of the outer layer etching process. The date code should consist of four digits. The first two digits shall represent the year and the last two digits shall represent the week of the year fabricated (i.e., March 17, 2006 will have a date code of 0611).

3.8.3 Lot Code Traceability

The supplier must be capable of providing upon request, traceability to raw material / each fabrication process used in a specific lot.

3.8.4 Logo Box/Solder Mask Coverage

The supplier may alter the solder mask artwork to allow solder mask coverage of the logo box.

3.9 CHARACTERISTIC IMPEDANCE

3.9.1 Specification and Tolerance Requirements

HED Engineering Group will design and define the impedance requirements. The impedance value and tolerance for the affected layers will be documented on the PCB drawing. The tolerance will be + 10% if not defined on the PCB drawing.

3.9.2 Supplier Responsibilities

The supplier must fabricate the PCB to match the impedance goal as defined on the drawing. The supplier is required to design a test coupon that will be included on the panelized frame (provided it does not interfere with other features within the location) or the supplier will provide a separate coupon that has been part of the supplier's panel. The following information will be included with the coupons:

- The supplier's name or UL logo
- The date code
- The HED part number with correct revision number
- A three-digit serial number on each coupon and PCB

The initial lot shall have 100% of the coupons tested by the supplier using Time Domain Reflectometry (TDR) test equipment. Test results and coupons from initial lot should be included in the First Article Inspection package. Subsequent shipments shall be tested per a sampling plan coordinated with Supplier Quality Assurance.

3.9.3 Coupon Requirements

Test coupons must model the construction and trace characteristics of the PCB. Test coupons may be designed per PCB or per panel. Coupons from subsequent lots must be supplied upon HED request.

3.10 CARBON INK

3.10.1 Material

Acceptable carbon ink material is Tamura MRX-713J-A that meets the following requirements:

- Resistivity: 30-40Ω/square/0.001"
- Thickness: 0.001" nominal.
- Appearance: Dark gray in color with no pin holes or discontinuities in the ink.

Carbon Ink shall be placed over solder mask over base copper except where a solder mask opening is provided for connection to the circuit copper. The carbon ink shall not extend beyond the boundaries of the base copper to prevent potential cracking and exposed copper.

No other carbon ink type may be used without HED Engineering authorization.

3.11 CLEANLINESS

3.11.1 Final Wash

All PCBs need to be washed after final part assembly/soldering and re-work (if needed).

Earlier washes are permitted.

3.11.2 Cleanliness Ratings

The following ratings must be met on both bare boards and assembled PCBs. Cleanliness testing is post Final Wash. After successful testing, boards may be conformal coated by the supplier or shipped to HED if conformal coating is not required.

Condition	Omega Meter	Ionograph	Zero Ion	ICOM 5000
Bare board	6	8.57	15.86	9.43
Assembled	14	20	37	22

Note: All units are in $\mu g / in^2$

3.12 CONFORMAL COATING

When applied, a minimum thickness of 0.005" over the entire coated region(s) is required.

HED Approved Coatings are:
Dow Corning 2577 LVOC
Dow Corning 1-2577
Dow Corning 2577

3.13 PACKAGING REQUIREMENTS

3.13.1 Method

PCBs shall be packaged to guarantee protection against corrosion, deterioration, abrasion, moisture absorption and any other physical damage.

3.13.2 Materials

Materials used for shipping must be free of contaminants. Slip sheets, when used, are to be sulfur free. Bags, when used, must be free of silicon, sulfur compounds, polysulfides and other ionic contaminants. Vacuum sealing of PCBs is recommended. Packaging

utilizing "peanuts" is not acceptable. Desiccant packs must not be positioned where they may cause obstruction to flat board storage. Improper location may cause board warp / twist in HED stock.

3.13.3 Packaging Requirements

When a number of small bundles are packed within a larger container, each bundle is to be marked separately with the part number, date code and quantity. Bundles containing PCBs that are not individually bagged shall be sealed in plastic.
Containers are to be corrugated fiberboard with a minimum of single wall (double-faced) construction.
Each container shall not have a gross weight exceeding forty (40) pounds.
The container will provide sufficient stacking strength to avoid crushing the contents by top loading of two (2) additional containers (three high stacking).

3.13.4 Supplier Stock

PCBs that are stored at the supplier's facility must meet the PCB age criteria and packaging requirements of this specification. Product shall be shipped using a First In, First Out (FIFO) system, to utilize oldest stock first.

3.13.5 Container Identification

Container identification is required to enhance receiving inspection / stocking functions. PCBs shipped against different purchase orders must be packaged in separate containers with each marked in a permanent manner with the following:

- Part number / revision number / PO number

- Quantity/Date Code(s) - To enhance inventory control, the container shall be marked with the date code. Containers having more than one date code must have each date code and quantity identified as follows :

Date Code 0301 = Qty. 20 Date Code 0305 = Qty. 15 Date Code 0308 = Qty. 5

- Packing list

3.13.6 PCB Age Criteria

All PCBs that are more than twelve (12) months old shall not be shipped unless they satisfy one of the following requirements:

1) Prior documented approval from HED
2) Product accompanied by test report verifying acceptable solderability in accordance with J-STD-003A requirements (Solderability Tests for Printed Circuit Boards).
3) Product has been "re-HASLed" (in this case, a new date code must be stamped near the original date code)

If a PO is mixed with product that is both more / less than 12 months age, the containers and packing slip must reflect the mix.

Immersion Silver (IAg) finished boards must be less than (3) months old when received at HED or PCB Assembly Manufacturer.